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|  |  |  |  | **Lesson Plan** |  |  |
| Name of Faculty | : | Rajesh Kumar |  |  |
| Discipline | : | Computer Engg |  |  |
| Semester | : |  3rd |  |  |
| Subject |  | : | Digital Electronics-I |  |  |
| Lesson Plan Duration : | 15 Weeks ( From July 2018 to November 2018 ) |
|  |  |  |  |  |  |  |
| **Week** |  |  |  | **Theory** |  | **Practical** |
|  |  | **Lecture** |  | **Topic** | **Pr** | **Topic** |
|  |  | **Day** | **(including assignment/test )** | **Day** |  |
|  |  |  |  |  |  |
| 1 | 1 | Introductiona) Define digital and analog signals and systems, difference between analog and digital signals | 1 | 1. Study of logic breadboard with verification of truth table for AND, OR, NOT, NAND, EX-OR, NOR gate |
| 2 | b) Need of digitization and applications of digital systems |
| 3 | Revision |
| 4 | Number Systemsa) Decimal, binary, octal, hexadecimal number systems |
| 2 | 5 | b) Conversion of number from one number system to another including decimal points | 2 | 2. Verification of NAND and NOR gate as universal gates |
| 6 | c) Binary addition, subtraction, multiplication, division,  |
| 7 | 1’s and 2’s complement method of subtraction |
| 8 | d) BCD code numbers and their limitations,  |
| 3 | 9 | addition of BCD coded numbers, conversion of BCD to decimal and vice-versa | 3 | 3. Construction of half-adder and full adder circuits using EX-OR and NAND gate and verification of their operation |
| 10 | e) Excess-3 code, gray code,  |
| 11 | binary to gray and gray to binary conversion |
| 12 | f) Concept of parity, single and double parity, error detection and correction using parity |
| 4 | 13 | Revision | 4 | 4. Verify the operation ofa) multiplexer using an IC |
| 14 | Revision |
| 15 | Logic Gatesa) Logic gates, positive and negative logic, pulse waveform, definition, |
| 16 | symbols, truth tables, pulsed operation of NOT, OR, AND, NAND,  |
| 5 | 17 | NOR, EX-OR, EX-NOR gates | 5 | 4. b) de-multiplexer using an IC |
| 18 | b) NAND and NOR as universal logic gates |
| 19 | Revision |
| 20 | Revision |
| 6 | 21 | Logic Simplification) a) Rules and laws of Boolean algebra, logic expression,  | 6 | Revision |
| 22 | Demorgan theorems, their proofb) Sum of products form (minterm), Product of sum form (maxterms), |
| 23 | simplification of Boolean expressions with the help of Rules and laws of Boolean algebra |
| 24 | c) Karnaugh mapping techniques upto 4 variables and their applications for simplification of Boolean expression |
| 7 | 25 | Revision | 7 | 5. a) Verify the operation of BCD to decimal decoder using an IC |
| 26 | Revision |
| 27 | Arithmetic Circuits a) Half adder, full adder circuits and their operation |
| 28 | b) Parallel binary adder, 2-bit and 4-bit binary full adder, block diagram, working |
| 8 | 29 | Revision | 8 | 5. b) Verify the operation of BCD to 7 segment decoder using an IC |
| 30 | Revision |
| 31 | Multiplexer/Demultiplexera) Basic functions, symbols and logic diagrams of 4-inputs and 8-inputs multiplexers, |
| 32 | b) Function/utility of 16 and 32 inputs multiplexers, |
| 9 | 33 | c) Realization of Boolean expression using multiplexer/demultiplexers | 9 | 6. Verify operation of SR, JK, D-flip-flop master slave JK filp-flop using IC |
| 34 | Revision |
| 35 | Revision |
| 36 | Decoders, Display Devices and Associated Circuits |
| 10 | 37 | a) Basic Binary decoder, 4-line to 16 line decoder circuit | 10 | Revision |
| 38 | b) BCD to decimal decoder, BCD to 7-segment decoder/driver, LED/LCD display |
| 39 | Revision |
| 40 | Revision |
| 11 | 41 | Encoders and Comparatorsa) Encoder, decimal to BCD encoder,  | 11 | 7. Verify operation of SISO, PISO, SIPO, PIPO shift register. (universal shift register) |
| 41 | decimal to BCD priority encoder, keyboard encoder |
| 43 | b) Magnitude comparators, symbols and logic diagrams of 2-bit and 4-bit, c) Comparators  |
| 44 | Revision |
| 12 | 45 | Revision | 12 | 8. Study of ring counter, Up/down counter |
| 46 | Latches and Flip-Flopsa) Latch, SR-latch, D-latch, Flip-flop, difference between latch and flip-flop |
| 47 | b) S-R, D flip-flop their operation using waveform and truth tables, race around condition |
| 48 | c) JK flip-flop, master slave and their operation using waveform and truth tables |
| 13 | 49 | Revision | 13 | 9. Construct and verify the operation of an asynchronous binary decade counter usingJK flip-flop |
| 50 | Revision |
| 51 | Countersa) Asynchronous counter, 4-bit Asynchronous counter, Asynchronous decade counter |
| 52 | b) Asynchronous counter, 4-bit synchronous binary counter, Asynchronous decade counter |
| 14 | 53 | c) Up/down Asynchronous counters, divide by N counter | 14 | 10. Testing of digital ICs using IC tester |
| 54 | MOD-3,MOD-5, MOD-7, MOD-12 counters |
| 55 | d) Ring counter, cascaded counter, counter applications |
| 56 | Shift Registersa) Shift registers functions, serial-in-serial out,  |
| 15 | 57 | serial-in-parallel-out, parallel-in-serial-out, parallel-in-parallel out | 15 | Revision |
| 58 | b) Universal shift register, shift register counter and  |
| 59 | applications of shift registers |
| 60 | Revision |